

What is claimed is:

1. A power-up circuit of a semiconductor memory device,  
comprising:

5       a power supply voltage level follower unit for providing  
a bias voltage which is linearly varied according to variation  
of a power supply voltage;

      a power supply voltage detection unit for detecting the  
variation of the power supply voltage to a predetermined  
10 critical voltage level in response to the bias voltage; and

      a reset prevention unit for canceling variation of the  
detection signal due to a power drop by delaying level  
transition of the detection signal according to decrease of  
the power supply voltage.

15

2. The power-up circuit as recited in claim 1, further  
comprising a buffer unit for outputting a power-up signal by  
buffering an output signal of the reset prevention unit.

20       3. The power-up circuit as recited in claim 1, wherein  
the reset prevention unit includes:

      a first pull-up means and a first pull-down means  
controlled by an output signal of the power supply voltage  
detection unit; and

25       a response delaying means for delaying an pull-up  
operation of the first pull-up means according to transition  
of the output signal of the power supply voltage detection

unit.

4. The power-up circuit as recited in claim 3, wherein the response delay means includes:

5 a delay unit for delaying the output signal of the power supply voltage detection unit by a predetermined time; and

a second pull-up means connected between the first pull-up means and a power supply voltage, and controlled by an output signal of the delay unit.

10

5. The power-up circuit as recited in claim 4, wherein the predetermined time for delaying the output signal of the power supply voltage detection unit in the delay unit is longer than a time that the detection signal is maintained in a logic low level due to the power drop.

15

6. The power-up circuit as recited in claim 4, wherein the reset prevention unit further includes an inverter connected to the first pull-up means and the first pull-down means.

20

7. The power-up circuit as recited in claim 4, wherein the first and second pull-up means are a PMOS transistor, and the pull-down means is an NMOS transistor.

25

8. The power-up circuit as recited in claim 4, wherein the power supply voltage level follower unit is provided

between the power supply voltage and a ground voltage, and includes a first and a second load elements configuring a voltage divider.

5           9. The power-up circuit as recited in claim 4, wherein the power supply voltage detection unit includes:

          a load element connected between the power supply voltage and a first node;

          an NMOS transistor which is connected between a ground  
10 voltage and the first node and whose gate receives a bias voltage; and

          an inverter, which is connected to the first node, for outputting the detection signal.

15           10. The power-up circuit as recited in claim 9, wherein the load element is a PMOS transistor which is connected between the power supply voltage and the first node, and whose gate is connected to the ground voltage.

20           11. The power-up circuit as recited in claim 2, wherein the buffer unit includes an inverter chain receiving an output signal of the reset prevention unit.